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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,032	08/10/2001	James S. Raitter	4539US (MUEI-0560.00/US)	5192

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EXAMINER
CHARIOUI, MOHAMED

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 08/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/928,032	RAITTER, JAMES S.
	Examiner	Art Unit
	Mohamed Charioui	2857

-- The MAILING DATE of this communication appears on the c ver sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-9, 18, 20-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Wilson et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claims 1, 3, 4, 8 and 9, Wilson et al. teach reading an ID code on the multi-die handling device (see col. 4, lines 15-43); retrieving a tray map file (i.e. lead frame codes) corresponding to the ID code; determining a tray matrix of the multi-die handling device (i.e. lot numbers); retrieving data from the tray map file (see col. 7, lines 22-39), the data comprising unique characters correlating to each semiconductor device

of the plurality of semiconductor devices; and marking each semiconductor device with the data (see col. 6, line 59 to col. 7, line 12 and col. 8, lines 6-31).

As per claims 18, 23, 25 and 26, Wilson et al. teach providing a multi-die handling device having a plurality of pockets therein in a matrix; placing at least one semiconductor device in at least one pocket of the multi-die handling device (see col. 6, line 59 to col. 7, line 12 and col. 9, lines 25-58); reading an ID code on the multi-die handling device (see col. 4, lines 15-43); retrieving a tray map file (i.e. lead frame) corresponding to the ID code; determining a tray matrix of the multi-die handling device (i.e. lot numbers); retrieving data from the tray map file (see col. 7, lines 22-39), the data comprising unique characters correlating to each semiconductor device of the plurality of semiconductor devices; and marking each semiconductor device with the data (see col. 8, lines 6-31).

As per claims 5, 6 and 22, Wilson et al. further teach that unique characters comprise test data extracted for at least one semiconductor device from the tray map file (see col. 7, lines 22-39).

As per claims 7 and 24, Wilson et al. further teach that semiconductor device each comprise a semiconductor device selected from the group consisting of Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Single In-Line Memory Modules (SIMMs), and Dual In-Line Memory Modules (DIMMs) (see col. 6, lines 25-58).

As per claims 20 and 21, Wilson et al. further teach that non-unique characters selected from the group consisting of semiconductor device data, date code, country code and company logo (see col. 7, lines 13-21).

Claim Rejections - 35 USC § 103

2. **Claims 2 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. in view of Lambert.

Wilson et al. teach the system as stated above except that the multi-die handling device comprises a JEDEC tray.

Lambert teaches this feature (see col. 2, line 54 to col. 3, line 15). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Lambert's teaching into Wilson et al.'s invention because JEDEC trays would stack a large number of IC devices. Therefore, the large batch of IC devices would be stored, scanned, tested, marked, processed and transported in a more efficient way.

3. **Claims 10, 11, 13-17, 27, 28, 30-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. in view of Beffa.

As per claims 10, 11, 16, 17, 27, 28, 33 and 34, Wilson et al. teach providing a plurality of carriers (i.e. lead frames), each carrier having a plurality of pockets therein in a matrix; assigning each carrier of the plurality of carriers an ID code (see col. 7, lines 12-39); placing each semiconductor device of the plurality of semiconductor devices in a pocket of the plurality of pocket locations (see col. 6, line 59 to col. 7, line 12 and col. 9, lines 25-58); testing each semiconductor device; generating a tray map file comprising

test data corresponding to each semiconductor device; storing the tray map file in association with the ID code of each carrier (see col. 7, lines 22-39); reading an ID code on a carrier (see col. 4, lines 15-43); retrieving a tray map file corresponding to the ID code; determining a tray matrix of the carrier; retrieving data from the tray map file (see col. 6, line 59 to col. 7, line 39); and marking each semiconductor device with the data of the plurality of devices with the corresponding test data(see col. 8, lines 6-31).

Wilson et al. fail to teach retrieving a plurality of semiconductor devices from a reject bin.

Beffa teaches this feature (see col. 3, lines 24-38). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Beffa's teaching into Wilson et al.'s invention because reject bins containing previously rejected IC's that would be retrieved and tested under relaxed testing standards. Therefore, the IC devices would be stored according to whether their test results pass the relaxed test standard. Furthermore, the IC devices that would pass the relaxed test standard would be recovered.

As per claims 13, 14, 30 and 31, Wilson et al. further teach that non-unique characters selected from the group consisting of semiconductor device data, date code, country code and company logo (see col. 7, lines 13-21).

As per claims 15 and 32, Wilson et al. further teach that semiconductor device each comprise a semiconductor device selected from the group consisting of Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor

devices, processor semiconductor devices, Single In-Line Memory Modules (SIMMs), and Dual In-Line Memory Modules (DIMMs) (see col. 6, lines 25-58).

4. **Claims 12 and 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson et al. in view of Beffa and Lambert.

Wilson et al. in view of Beffa teach the system as stated above except that the multi-die handling device comprises a JEDEC tray.

Lambert teaches this feature (see col. 2, line 54 to col. 3, line 15). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Lambert's teaching into Wilson et al. in view of Beffa's teaching because JEDEC trays would stack a large number of IC devices. Therefore, the large batch of IC devices would be stored, scanned, tested, marked, processed and transported in a more efficient way.

Prior art

5. The prior art made record and not relied upon is considered pertinent to applicant's disclosure:

Anderson ['838] discloses pin array set-up device.

Corley et al. ['578] disclose integral semiconductor wafer map recording.

Jones et al. ['923] disclose metod for continuous, non lot-based integrated circuit manufacturing.

Weber ['395] discloses method and apparatus for maintaining test data during fabrication of a semiconductor wafer.

Soh et al. [2002/0066694] disclose tray for storing semiconductor chips.

Peterson et al. [2002/0057963] disclose methods and apparatus for retaining a tray stack having a plurality of trays for carrying microelectronic devices.

Stuckey et al. ['373] disclose electronic device handling system and method.

Farnworth et al. ['137] disclose system and method for dicing semiconductor components.

Gune et al. ['531] disclose system for batching integrated circuits in trays.

Banks et al. ['722] disclose method for assembling an integrated circuit chip package having an underfill material between a chip and a substrate.

Long et al. ['766] disclose semiconductor device package and method of making such a package.

Morton ['413] discloses apparatus for tracking integrated circuit devices.

Littlebury ['988] discloses method for assembling, testing, and packaging integrated circuits.

Fukasawa ['472] discloses test handler for semiconductor devices.

Canella ['270] discloses method of efficiently laser marking singulated semiconductor devices.

Anderson ['204] discloses die sorter.

Contact information

6. Any inquiry concerning this communication from examiner should be directed to Mohamed Charioui whose telephone number is 703 605-4362. The examiner can normally be reached Monday to Friday 9 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached at 703 308-1677. The fax phone number for the organization where this application is assigned is 703 305-3431.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose number is 703 308-0956.

Mohamed Charioui

8/9/03

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800